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CARTER III, ROBERT E	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/522,847	Applicant(s) EDWARDS ET AL.
	Examiner Robert E. Carter	Art Unit 2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 05 December 2007.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1,2 and 4-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-2, 4-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on 12/05/2007 has been entered and considered by the examiner.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites the limitation "wherein the capacitive connection comprises" in lines 8 and 9. There is insufficient antecedent basis for this limitation in the claim because there is no previous instance of a capacitive connection in claim 10.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-13,15-18, and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murai et al. (JP 2001-305511) in view of Akimoto et al. (US Publication # 2002/0084967).

As for claim 1, Murai et al. (Figs. 1, 5, 6) discloses:

A device comprising an array of pixels (1002), *each pixel including a pixel element* (1102) *and being associated with a switching circuit* (11, 12, 13, 14), *wherein the switching circuit is for selectively routing one of at least two inputs* (3, 1012) *to the pixel element, comprising at least first* (13) *and second switching transistors* (14) *connected between a respective one of the at least two inputs and the pixel element,*
wherein each switching transistor is controlled by a data signal applied to the gate of the transistor, wherein the data signal for each switching transistor is routed to the gate of the switching transistor with predetermined timing determined in dependence on the data waveform of at least one of the inputs, and

The gates of switching transistors 13 and 14 are both connected to the output of transistor 11. The input of transistor 11 is the data signal from the data line 1. The gate of transistor 11 is controlled by input line 51. Transistors 13 and 14 are complementary

such that when one is off, the other is on and vise versa. Therefore transistors 13 and 14 are controlled by the data signal routed to their gates through transistor 11 with predetermined timing in dependence on the data waveform of input line 51.

Murai et al. further teaches the switching transistors having a common output node (the node connecting transistors 13, 14, and 15).

Murai et al. does not teach a capacitive connection between the gate and common output of the switching transistors.

In the same field of endeavor (i.e. in-pixel driver circuits) Akimoto et al. (Fig. 25) discloses a pixel circuit with a bootstrap capacitor (88) between the gate and output of one of the switching transistors [0204].

The combination of Murai et al. and Akimoto et al. teaches:

wherein a capacitive connection (88) *is provided between the gate of at least one of the switching transistors and a common output node* (node connecting transistors 13, 14, and 15) *of the switching transistors.*

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add the bootstrap capacitor in Akimoto et al. to at least one of the switching transistors in Murai et al. to reduce the power consumption of the liquid crystal display [0001].

As for claim 2, Murai et al. as modified by Akimoto et al. teaches:

wherein the data signal for each switching transistor is routed to the gate of the switching transistor by a transfer switch (Murai et al., 11) *which controls the timing of application of the data signal for each switching transistor, and*

In Murai et al. the gates of switching transistors 13 and 14 are both connected to the output of transistor 11. The input of transistor 11 is the data signal from the data line 1. The gate of transistor 11 is controlled by input line 51. Transistors 13 and 14 are complementary such that when one is off, the other is on and vise versa. Therefore transistors 13 and 14 are controlled by the data signal routed to their gates through transistor 11 with predetermined timing in dependence on the data waveform of input line 51.

wherein a capacitive connection (Akimoto et al., 88) *is provided between the gate of each switching transistor and the common output node* (because the gates of transistors 13 and 14 are connected together, the capacitive connection 88 of claim 1 is between the gate of each switching transistor and the common output node).

As for claim 4, Murai et al. as modified by Akimoto et al. teaches:

wherein the gates of the first and second switching transistors are connected together (In Murai et al. the gates of transistors 13 and 14 are both connected to the output of transistor 11) *and the capacitive connection comprises a capacitor* (Akimoto et al., 88) *connected between the gates and the common output node* (The capacitive connection 88 in the rejection of claim 1 is a capacitor).

As for claim 5, Murai et al. teaches:

wherein the first switching transistor is an n-type transistor (13) *and the second switching transistor is a p-type* (14) *transistor* [0031].

As for claim 6, Murai et al. as modified by Akimoto et al. teaches:

wherein the capacitive connection comprises a respective capacitor (88) *connected*

between the gate of each switching transistor and the common output node (The capacitive connection 88 in the rejection of claim 1 is a capacitor. Furthermore, because the gates of transistors 13 and 14 are connected together, the capacitive connection 88 of claim 1 is between the gate of each switching transistor and the common output node).

As for claim 12, Murai et al. teaches:

an active matrix liquid crystal display device ([0011] an active matrix display being one that contains TFTs in the pixel area) *in which the pixel elements comprise liquid crystal cells* [0004], *each pixel comprising the switching circuit for routing one of two voltage drive* levels (3, 1012) to *the pixel element.*

As for claim 13, Murai et al. teaches:

a first selection switch (15) *between the common output node of the switching circuit and the liquid crystal cell of the pixel; and*

a second selection switch (1101) *between an analogue pixel data* line (1) and *the liquid crystal cell of the pixel.*

As for claim 15, Murai et al. teaches:

wherein the control signal for selecting which one of the two voltage drive levels is to be routed to the pixel element is provided on the analogue pixel data line.

The gates of switching transistors 13 and 14 are both connected to the output of transistor 11. The input of transistor 11 is the control signal from the analogue pixel data line 1. Transistors 13 and 14 are complementary such that when one is off, the other is on and vise versa. Therefore one of the two transistors 13 and 14, and thus one of the

two voltage drive levels, is routed to the pixel element based on the control signal provided on the analogue pixel data line.

As for claim 16, Murai et al. as modified by Akimoto et al. teaches:

wherein the data signal for each switching transistor is routed to the gate of the switching transistor by a transfer switch (Murai et al., 11) *which controls the timing of application of the data signal for each switching transistor, and wherein the transfer switch is provided between the analogue pixel data line and the gates of the first and second switching transistors, and*

In Murai et al. the gates of switching transistors 13 and 14 are both connected to the output of transistor 11. The input of transistor 11 is the data signal from the data line 1. The gate of transistor 11 is controlled by input line 51. Transistors 13 and 14 are complementary such that when one is off, the other is on and vise versa. Therefore transistors 13 and 14 are controlled by the data signal routed to their gates through transistor 11 with predetermined timing in dependence on the data waveform of input line 51.

wherein a capacitive connection (Akimoto et al., 88) *is provided between the gate of each switching transistor and the output of each switching transistor* (because the gates of transistors 13 and 14 are connected together, the capacitive connection 88 of claim 1 is between the gate of each switching transistor and the common output node).

As for claim 17, Murai et al. teaches:

a first selection switch (15) *between the output of the at least one of the switching transistors and the liquid crystal cell of the pixel; and*

a second selection switch (1101) *between an analogue pixel data line and the liquid crystal cell of the pixel.*

As for claim 18, Murai et al. teaches:

wherein the second selection switch comprises the other of the first and second switching transistors.

Since Murai et al. teaches both the second switching transistor 14 and the second selection switch 1101 in the same circuit, and because transistor 1101 has all of the functionally of the second switching transistor 14 as defined in preceding claims upon which claim 18 depends, defining the second selection switch as also being the second switching transistor of claim 1 is simply a matter of renaming a pre-existing part

As for claim 10, Murai et al. teaches:

A device comprising an array of pixels (1002), *each pixel including a pixel element* (1102) *and being associated with a switching circuit* (11, 12, 13, 14), *wherein the switching circuit is for selectively routing one of at least two inputs* (3, 1012) *to the pixel element, comprising at least first* (13) *and second switching transistors* (14) *connected between a respective one of the at least two inputs and the pixel element,*

wherein each switching transistor is controlled by a data signal applied to the gate of the transistor, wherein the data signal for each switching transistor is routed to the gate of the switching transistor with predetermined timing determined in dependence on the data waveform of at least one of the inputs, and

The gates of switching transistors 13 and 14 are both connected to the output of transistor 11. The input of transistor 11 is the data signal from the data line 1. The gate of transistor 11 is controlled by input line 51. Transistors 13 and 14 are complementary such that when one is off, the other is on and vise versa. Therefore transistors 13 and 14 are controlled by the data signal routed to their gates through transistor 11 with predetermined timing in dependence on the data waveform of input line 51.

the device further comprising n inputs, and comprising first to nth switching transistors connected between a respective one of the n inputs and one of two intermediate outputs (node between transistors 13 and 61, node between transistors 14 and 62), *and wherein the data signals for each switching transistor are selected such that half of the switching transistors are turned on to route a first selected input to one intermediate output and to route a second selected input to the other intermediate output.*

The gates of switching transistors 13 and 14 are both connected to the output of transistor 11. The input of transistor 11 is the data signal from the data line 1. Transistors 13 and 14 are complementary such that when one is off, the other is on and vise versa. Therefore transistors 13 and 14 are controlled by the data signal routed to their gates through transistor 11 such that half of the switching transistors are turned on to route a first selected input to one intermediate output and to route a second selected input to the other intermediate output.

Murai et al. further teaches the switching transistors having a common output node (the node connecting transistors 13, 14, and 15).

Murai et al. does not teach a capacitive connection between the gate and common output of the switching transistors.

In the same field of endeavor (i.e. in-pixel driver circuits) Akimoto et al. (Fig. 25) discloses a pixel circuit with a bootstrap capacitor (88) between the gate and output of one of the switching transistors [0204].

The combination of Murai et al. and Akimoto et al. teaches:

wherein the capacitive connection comprises a respective capacitor (88) *connected between the gate of each switching transistor and an output* (node connecting transistors 13, 14, and 15) *of the switching circuit,* (because the gates of transistors 13 and 14 are connected together, the capacitive connection 88 of claim 1 is between the gate of each switching transistor and their common output node).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add the bootstrap capacitor in Akimoto et al. to at least one of the switching transistors in Murai et al. to reduce the power consumption of the liquid crystal display [0001].

As for claim 7, Murai et al. teaches:

comprising n inputs (3, 1012, 1), *where n is greater than 2, and comprising first to nth switching transistors* (13, 14, 1101) *connected between a respective one of the n inputs and the pixel element, and wherein the data signals for each switching transistor are selected such that an individual one of the switching transistors is turned on to route the respective input to the pixel element.*

As for claim 8, Murai et al. teaches:

wherein at least one of the switching transistors is n-type (13) *and at least one of the switching transistors in p-type* (14), [0031].

As for claim 9, Murai et al. as modified by Akimoto et al. teaches all the limitations of claim 7.

Murai et al. does not teach all the switching transistors being the same polarity type.

Akimoto et al. teaches a pixel circuit where all of the transistors are the same polarity type (All of the transistors in Fig. 25 of Akimoto et al. are of the same type).

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to make all the switching transistors in Murai et al. the same polarity type because Applicant has not disclosed that making all the switching transistors the same polarity type provides an advantage, is used for a particular purpose, or solves a stated problem. Furthermore, one of ordinary skill in the art would have expected Applicant's invention to perform equally well with either multiple transistor polarity types as taught by Murai et al., or the claimed single polarity type because the switching transistors in either circuit would perform the same function of switching between the four voltage levels.

Therefore, it would have been an obvious matter of design choice to modify Murai et al. to obtain the invention as specified in claim 9.

As for claim 11, Murai et al. teaches:

further comprising a switching circuit (61, 62) *for selectively routing one of the intermediate outputs to the pixel element.*

As for claim 20, this claim differs from claims 1-2 only in that claim 20 is a method whereas claims 1-2 is an apparatus. Thus claim 20 is analyzed as previously discussed with respect to apparatus claims 1-2 above.

However, claim 20 also includes the limitations of turning on one transistor while turning off the other transistor, and controlling the timing such that the capacitive connection reduces the voltage swing.

Murai et al. teaches:

to turn on a selected one of the first and second switching transistors and turn off the other of the first and second switching transistor, thereby routing the respective input to the pixel element,

The gates of switching transistors 13 and 14 are both connected to the output of transistor 11. The input of transistor 11 is the data signal from the data line 1. Transistors 13 and 14 are complementary such that when one is off, the other is on and vise versa. Therefore transistors 13 and 14 are controlled by the data signal routed to their gates through transistor 11 such that when one is on, the other is off and vice versa, thereby routing the respective input to the pixel element.

Murai et al. does not teach the capacitive connection reducing the required voltage swing in the data signal.

In the same field of endeavor (i.e. in-pixel driver circuits) Akimoto et al. (Fig. 25) teaches:

wherein the timing is controlled such that the capacitive connection reduces the required voltage swing in the data signal between that required to turn on and turn off a switching transistor (Akimoto et al. [0204]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add the bootstrap capacitor operated such that it reduces the required voltage swing in the data signal in Akimoto et al. to at least one of the switching transistors in Murai et al. to reduce the power consumption of the liquid crystal display [0001].

As for claim 21, Murai et al. teaches:

in a first mode (Fig. 3), *switching analogue pixel drive signals* [Fig. 3, (b)] *to each pixel of the display; and*

in a second mode (Fig. 4), *routing one of two pixel drive signals* [Fig. 4, (b)] *on respective inputs to each pixel of the display, the routing for each pixel in the second mode using the method of claim 20.*

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murai et al. in view of Akimoto et al. as applied to claims 1, 12-13 above, and further in view of Murai (PCT Publication # WO01/40857) using the US application publication # 2002/0158993 as the English translation (henceforth referred to as Murai '993).

As for claim 14, Murai et al. as modified by Akimoto et al. teaches all the limitations of claim 13.

However they do not teach the two voltage levels for driving the liquid crystal cell to a black and a white state.

In the same field of endeavor (i.e. in-pixel LCD drivers) Murai '993 discloses: *wherein the two voltage drive levels comprise voltages for driving the liquid crystal cell to a black and a white state* [0046].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the voltage drive levels in Murai '998 in the LCD display of Murai et al. for driving the display to a black and a white state to reduce power consumption without lowering display quality [0006].

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murai et al. in view of Akimoto et al. as applied to claims 1, 12, 17-18 above, and further in view of Senda et al. (US Patent # 5,105,288).

As for claim 19, Murai et al. as modified by Akimoto et al. teaches: *wherein in a first mode* (Fig. 4), *the second selection switch* **is off**, *and in a second mode* (Fig. 3) *the second selection switch provides an analogue pixel signal* [Fig. 3(b)] *from the analogue pixel data line to the liquid crystal cell.*

Murai et al. as modified by Akimoto et al. does not teach a first mode where the second selection switch provides one of two digital pixel signals from the analogue pixel data line to the liquid crystal cell

In the same field of endeavor (i.e. in-pixel LCD drivers) Senda et al. (Figs. 1, 6) discloses:

wherein in a first mode (5 on, 8m on), *the second selection switch* (5) *provides one of two digital pixel signals* (Fig. 6) *from the analogue pixel data line* (4m) *to the liquid crystal cell* (C11), (Col. 3, lines 55-57, Col. 5, lines 36-41).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the digital pixel signal in Senda et al. on the analog pixel data line of Murai et al. to eliminate unevenness in the display and suppress leakage light (Senda et al. Col. 5, lines 41-48).

Response to Arguments

9. Applicant's arguments filed 12/05/2007 have been fully considered but they are not persuasive.

As for the 35 U.S.C. §l03(a) rejections of claims 1-13, 15-18 and 20-21, applicant argues:

"Transistor 87 is employed as a rewrite switch which is used to refresh the pixel without reusing the signal line (see FIG. 23 and the accompanying text). The rewrite transistor is employed for a completely different purpose from the present claim."

However, The functionality of transistor 87 is irrelevant because transistors with the correct functionality are already taught by Murai et al. Akimoto et al. is solely relied upon to teach applying a bootstrapping capacitor between the gates and common output of the transistors in Murai et al.

Applicant further argues:

"The rewrite switch (transistor) 87 of Akimoto includes a bootstrapped capacitor to store energy to preserve the pixel signal, and not to provide a single data signal that can be applied to two switching transistors to simultaneously switch one transistor on and the other off."

The examiner disagrees.

Applicant's abstract states:

"a capacitive connection is provided between the gate of at least one of the switching transistors and an output of the switching transistor. This enables a reduction in the data voltage range which is required to ensure that the switching transistors switch correctly, using a bootstrapping technique"

Paragraph [0204] of Akimoto et al. states:

"The gate voltage of the rewrite switch 87 is +5V. In practice, though it is assumed that the gate voltage is reduced down to approximately +2V due to the leak in DRAM, the rewrite switch 87 is turned on and the source voltage rises up to 5V like the drain voltage even in the case of the figure. This is because the gate voltage rises up approximately to 10V due to the bootstrap capacitance 88 formed between the source and the gate."

In both of these instances, the bootstrapping capacitor increases the voltage at the gate of the transistor to ensure proper switching when the gate signal voltage is lowered. This is what a bootstrapping capacitor does.

Therefore, the bootstrapping capacitor in Akimoto et al. operates in the same fashion as the bootstrapping capacitor in applicant's invention.

Applicant further argues:

"The Examiner stated that items 61 and 62 of Murai teach the intermediate outputs. Item 61 is a transistor in FIG. 6 of Murai but does not teach or suggest an intermediate output as recited in claim l0. Further, item 62 was not found in the FIGS. of Murai. In fact, no similar structure has been found in either Murai or Akimoto."

However, both item 61 and item 62 appear in Fig. 5 of Murai et al. Furthermore, it is the inputs to transistors 61 and 62 that correspond to the intermediate outputs of claim 10. The node between transistors 13 and 61 is a first intermediate output, and the node between transistors 14 and 62 is a second intermediate output. Therefore, Murai et al. teaches the intermediate outputs of claim 10.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Carter whose telephone number is 571-270-3006. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

REC

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